**REMARKS**

Claims 1-4, 10-13, 15, 19-21, and 24 are pending in the present application. Claims 1, 15 and 19 have been amended. Accordingly, claims 1-4, 10-13, 15, 19-21, and 24 remain pending in the application.

Claims 15 and 19 are objected to for informalities. Claims 15 and 19 have been amended to overcome the objection.

Claim 1 has been amended to correct a typographic error.

Claims 1-4, 10-13, 15, 19-21, and 24 stand rejected under 35 U.S.C. 103 as being unpatentable over Arimilli et al. (U.S. Patent Number 6,480,975, hereinafter "Arimilli '975") in view of Arimilli et al. (U.S. Patent Number 5,867,511, hereinafter "Arimilli '511"). Applicant respectfully traverses this rejection.

In addition to the Applicant's arguments made in the Office action Response dated April 11, 2005, Applicant makes the following additional arguments to further highlight why the application is in condition for allowance.

The Examiner asserts that the combination of Arimilli '975 and Arimilli '511 teach Applicant's invention. Applicant respectfully disagrees with the Examiner's characterization of Arimilli '975 and Arimilli '511 and his application of the cited art to Applicant's claims.

The Examiner acknowledges Arimilli '975 does not teach generating a cache miss in response to a request to access the directory cache. However, the Examiner asserts Arimilli '511 teaches this feature.

However, to summarize what was stated in Applicant's previous Response to Office action dated April 11, 2005, it appears that Arimilli '975 teaches detecting and

correcting certain classes of errors on the fly with a retry circuit and an ECC circuit, and if a certain uncorrectable classes of errors are detected, halting the processor.

It appears that Arimilli '511 teaches being able to overcome cache defects within a processor by never again using the defective cache line and permanently causing a cache miss in response to an access request to a bad cache line by using a repair mask. The repair mask functionally bypasses accesses by "keeping a defective cache line from ever indicating a cache hit and keeping a defective cache line from ever being chosen as a victim." (*See* col. 7, lines 11-14) Arimilli '511 also teaches testing the cache during manufacturing and at boot-up and updating the repair mask as needed.

Applicant submits this is in contrast to Applicant's invention as claimed.

The Examiner disagrees with Applicant in the Response to Arguments section of the present Office action. Specifically, the Examiner disagrees with Applicant's assertion that Arimilli teaches permanently causing a cache miss to an access to a bad cache line. In response, Applicant respectfully redirects the Examiner to col. 7 line 65 through col. 8, line 1, wherein Arimilli '511 discloses

> "Once the repair mask entry has been set, **any future accesses** to that cache line will be forced by the repair mask **to see a miss on that line**, and the line would **never** be re-used (victimized)." (Emphasis added)

In regard to the Examiner's assertion that the retry circuit allowing an ECC circuit to correct the problem, is analogous to Applicant's "servicing the directory cache in response to testing dynamically restoring the storage unit in response to testing the storage device"; Applicant again respectfully disagrees with the Examiner's piecewise application of the art to the Applicant's claims. Specifically, although the ECC circuit does try to correct errors in the data on the fly, as do most ECC type circuits, Applicant notes, the ECC circuit does not repair (i.e., service) the defective cache or portion thereof. To the contrary, it is well known that ECC circuits detect and/or correct the data that they operate on, depending on the class of error that is present. Furthermore, the retry and

ECC circuits of Arimilli do not take the cache offline to perform their operations as recited in Applicant's claim 1.

Thus, Applicant submits Arimilli '511 clearly teaches away from Applicant's claimed invention, since Applicant's invention is directed toward taking the directory cache offline for testing during continued operation of the domain in response to detecting an uncorrectable error, requesting service of the directory cache, and returning the directory cache to an online status in response to the service.

Applicant therefore submits neither Arimilli '975 nor Arimilli '511, taken singly or in combination, teach or suggest "while the system is in operation: testing the at least a portion of the directory cache while the at least a portion of the directory cache is offline based on determining that the error is uncorrectable," nor "servicing the at least a portion of the directory cache in response to testing the directory cache," nor "dynamically placing the allowing access to the at least a portion of the directory cache in response to servicing the at least a portion of the directory cache" as recited in Applicant's claim 1. (Emphasis added)

Accordingly, Applicant submits claim 1, along with its dependent claims, is believed to patentably distinguish over Arimilli '975 in view of Arimilli '511 for the reasons given above.

Applicant's independent claims 10 and 20 recite features that are similar to the features recited in claim 1. Thus, Applicant submits claims 10 and 20, along with their respective dependent claims, patentably distinguish over Arimilli '975 in view of Arimilli '511 for at least the reasons given above.

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-55600/SJC.

Respectfully submitted,

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